



2N7000 2N7002

N-channel 60V - 1.8Ω - 0.35A - SOT23-3L / TO-92
STripFET™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
2N7000	60V	<5Ω (@10V)	0.35
2N7002	60V	<5Ω (@10V)	0.20

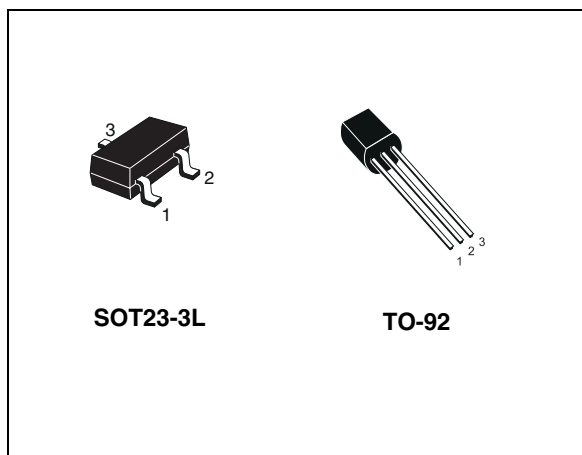
- Low Q_g
- Low threshold drive

Description

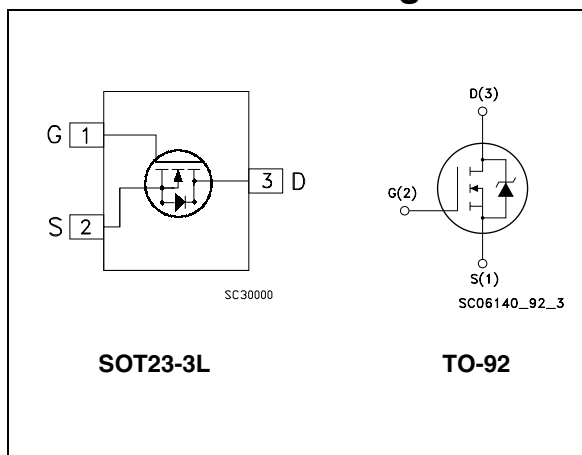
This MOSFET is the second generation of STMicroelectronics unique “Single Feature Size™” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
2N7000	2N7000G	TO-92	Bulk
2N7002	STN2	SOT23-3L	Tape & reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuit	9
4	Package mechanical data	10
5	Revision history	13

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-92	SOT23-3L	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	60		V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)	60		V
V_{GS}	Gate- source voltage	± 18		V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	0.35	0.20	A
$I_{DM}^{(1)}$	Drain current (pulsed)	1.4	1	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	1	0.35	W

1. Pulse width limited by safe operating area

Table 2. Thermal data

	Parameter	TO-92	SOT23-3L	Unit
		$R_{thj-amb}$	Thermal resistance junction-ambient max	
T_J	Operating junction temperature	- 55 to 150		$^\circ\text{C}$
T_{stg}	Storage temperature			

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	60			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$ $V_{DS} = \text{max rating},$ $T_C = 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 18V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	2.1	3	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 0.5A$ $V_{GS} = 4.5V, I_D = 0.5A$		1.8 2	5 5.3	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10V, I_D = 0.5A$		0.6		S
C_{iss}	Input capacitance	$V_{DS} = 25V, f = 1MHz,$ $V_{GS} = 0$		43		pF
C_{oss}	Output capacitance			20		pF
C_{rss}	Reverse transfer capacitance			6		pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30V, I_D = 0.5A$ $R_G = 4.7\Omega, V_{GS} = 4.5V$ (see Figure 15)		5		ns
t_r	Rise time			15		ns
$t_{d(off)}$	Turn-off delay time			7		ns
t_f	Fall time			8		ns
Q_g	Total gate charge	$V_{DD} = 30V, I_D = 1A,$ $V_{GS} = 5V$ (see Figure 16)		1.4	2	nC
Q_{gs}	Gate-source charge			0.8		nC
Q_{gd}	Gate-drain charge			0.5		nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				0.35 1.40	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 1A, V_{GS} = 0$			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 1A, di/dt = 100A/\mu s,$ $V_{DD} = 20V, T_j = 150^\circ C$ (see Figure 17)		32 25 1.6		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-92

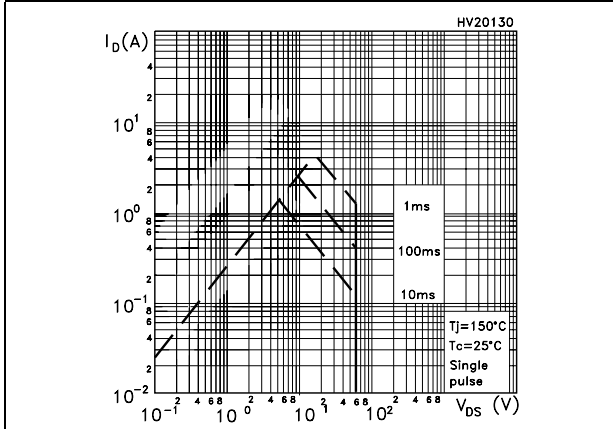


Figure 2. Thermal impedance for TO-92

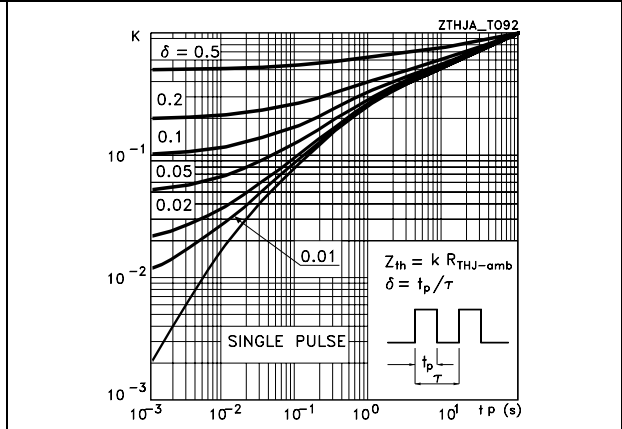


Figure 3. Safe operating area for SOT23-3L

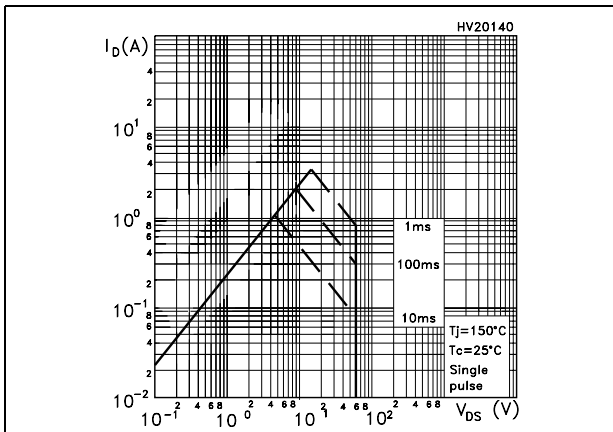


Figure 4. Thermal impedance for SOT23-3L

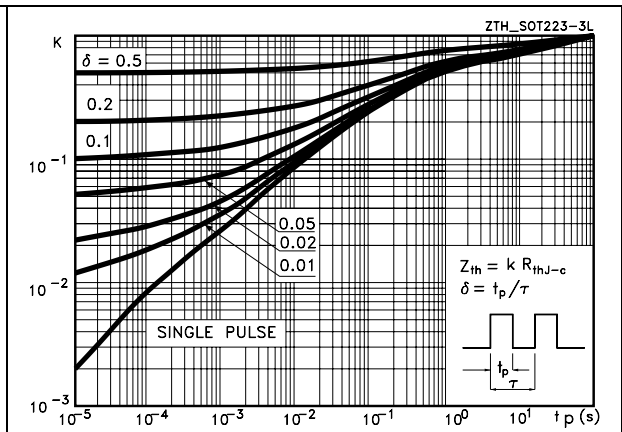


Figure 5. Output characteristics

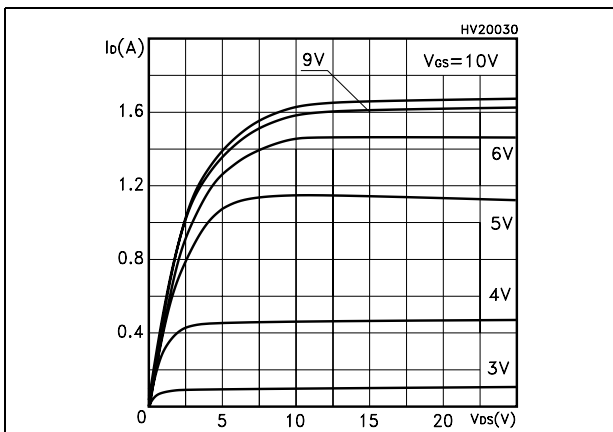


Figure 6. Transfer characteristics

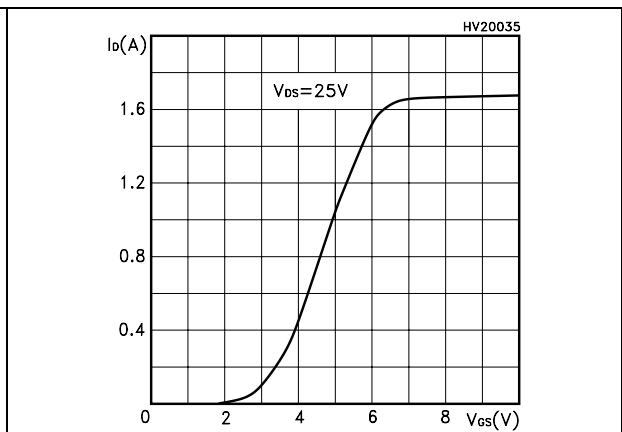


Figure 7. Transconductance

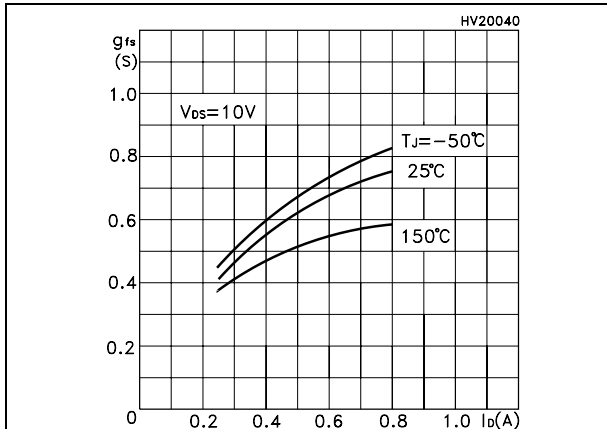


Figure 8. Static drain-source on resistance

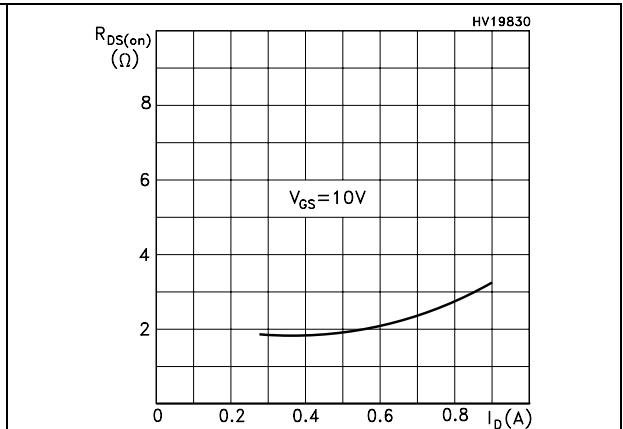


Figure 9. Gate charge vs gate-source voltage

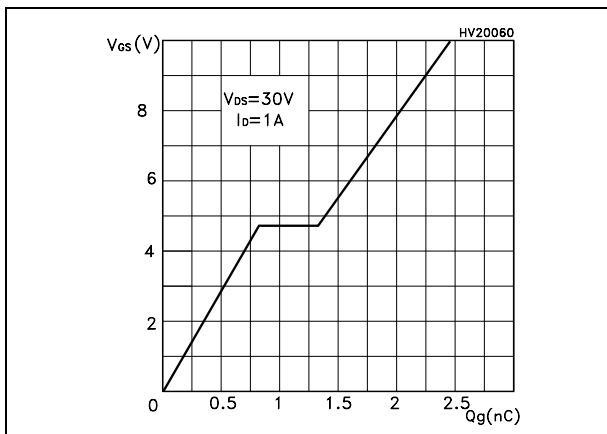


Figure 10. Capacitance variations

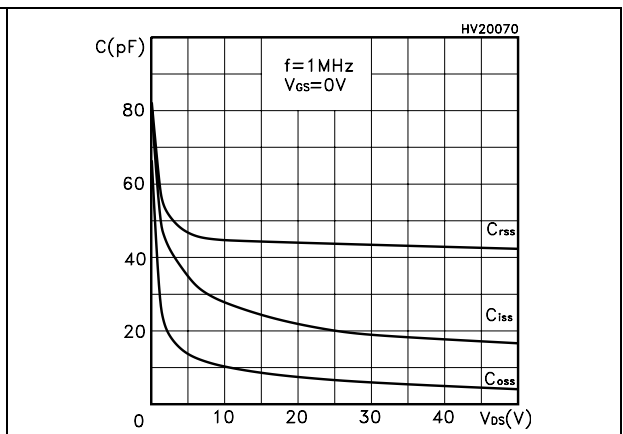


Figure 11. Normalized gate threshold voltage vs temperature

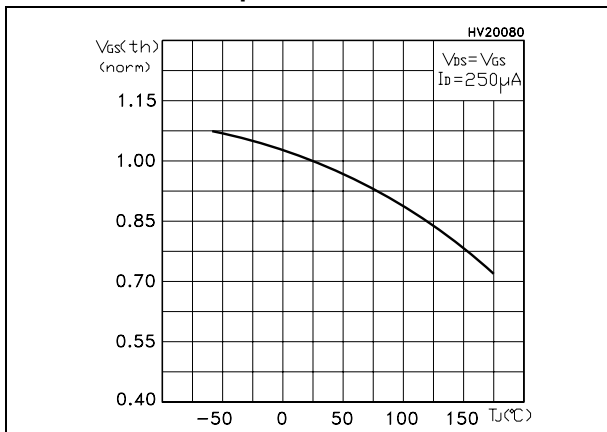


Figure 12. Normalized on resistance vs temperature

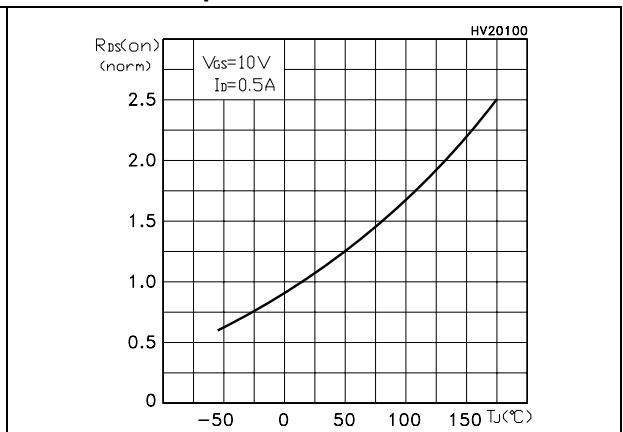


Figure 13. Source-drain diode forward characteristics

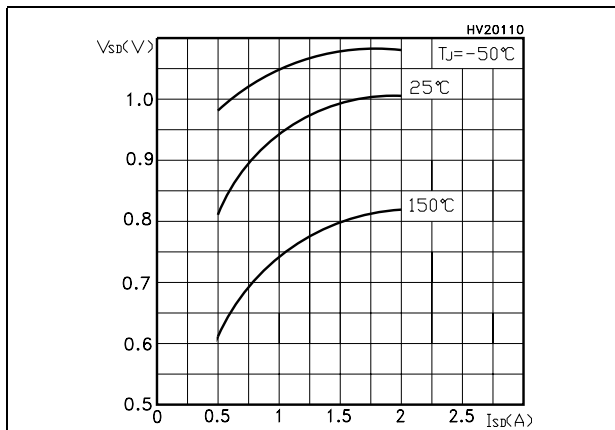
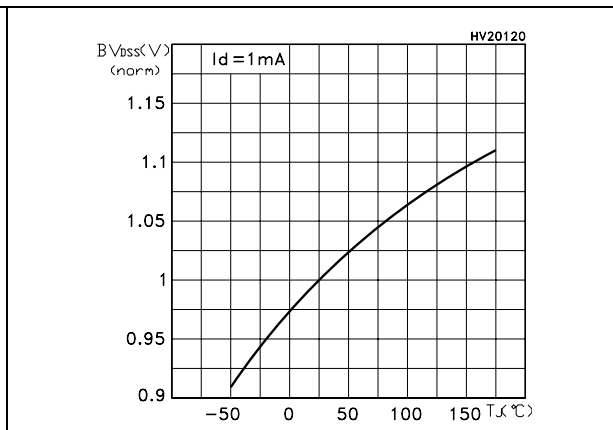


Figure 14. Normalized B_{VDSS} vs temperature



3 Test circuit

Figure 15. Switching times test circuit for resistive load

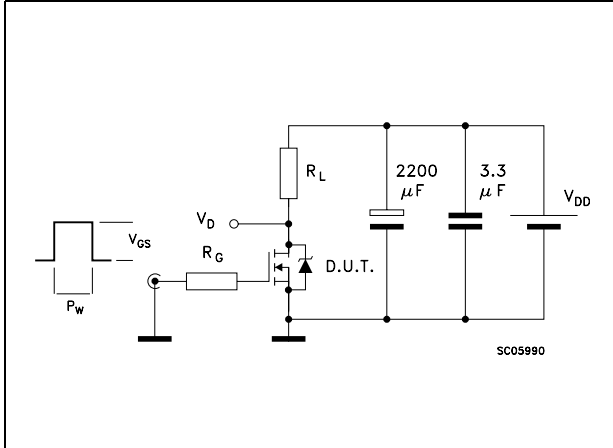


Figure 16. Gate charge test circuit

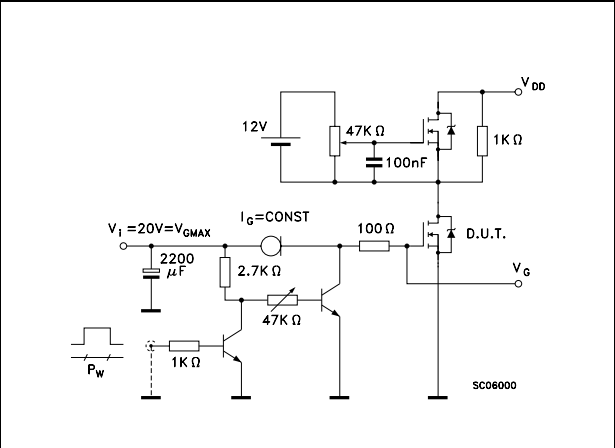


Figure 17. Test circuit for inductive load switching and diode recovery times

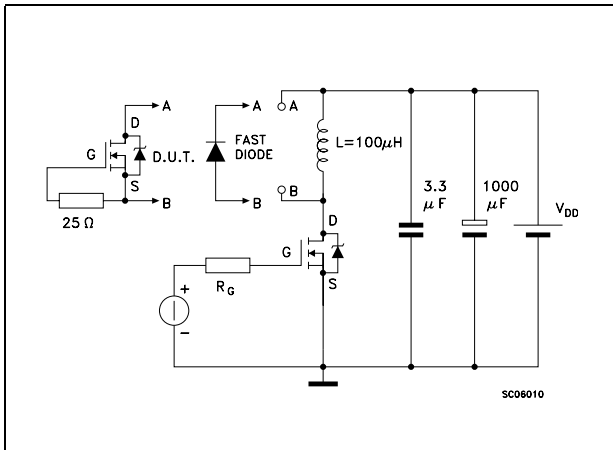


Figure 18. Unclamped Inductive load test circuit

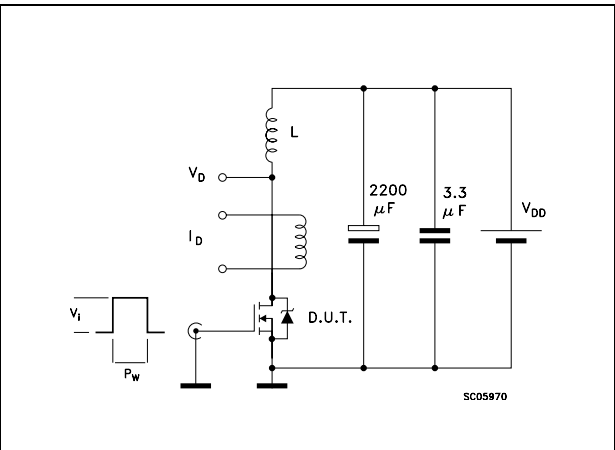


Figure 19. Unclamped inductive waveform

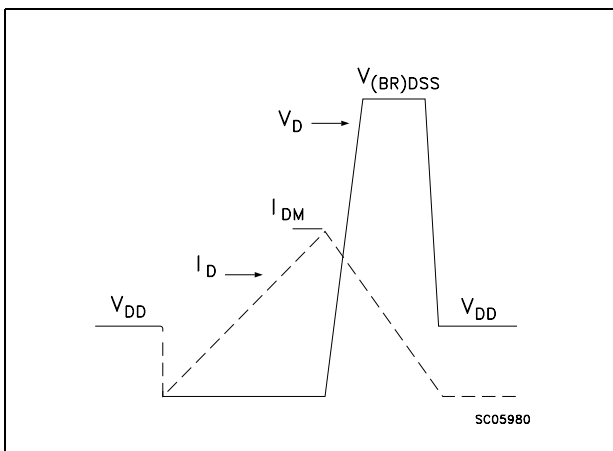
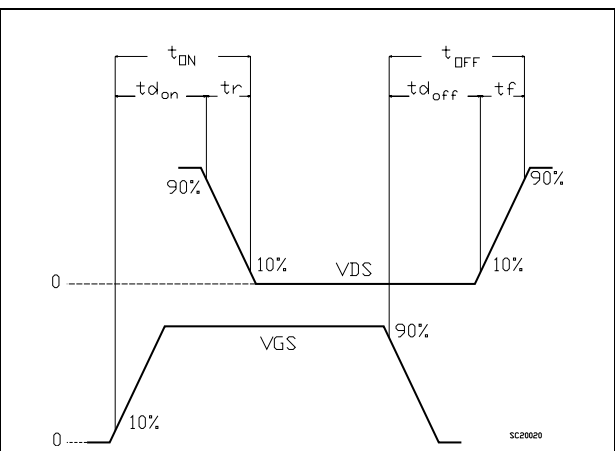


Figure 20. Switching time waveform

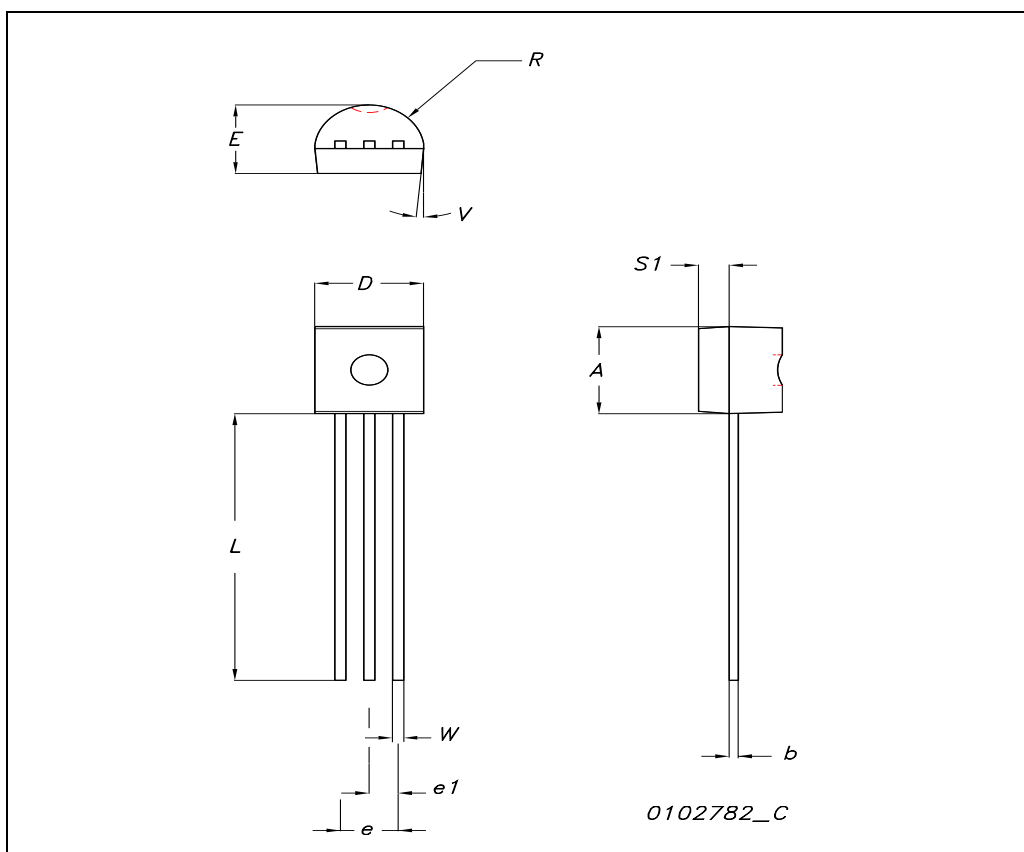


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

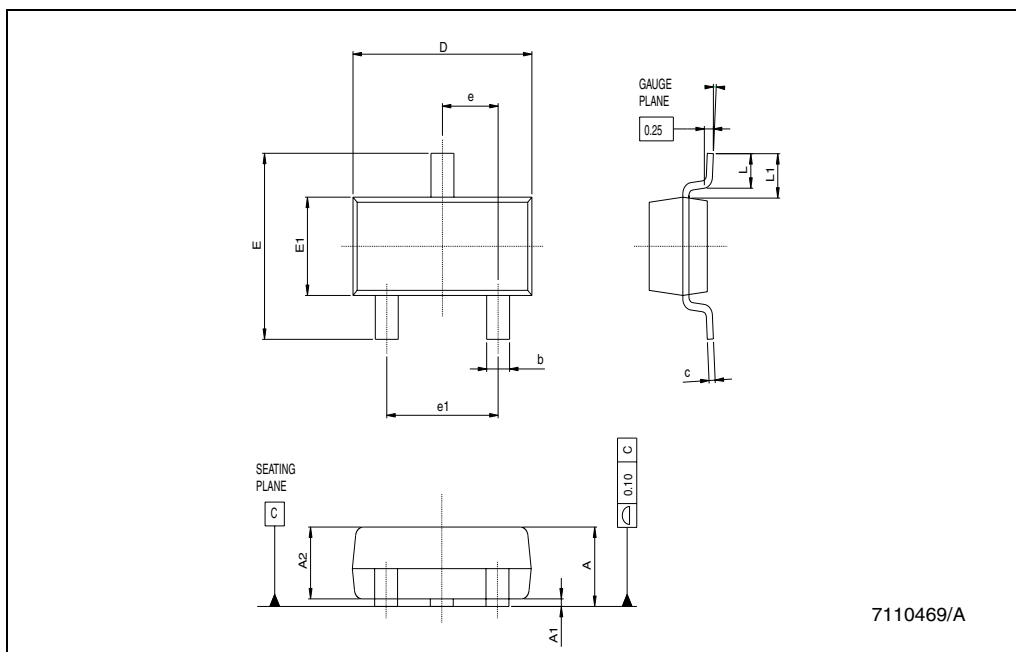
TO-92 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.32		4.95	0.170		0.194
b	0.36		0.51	0.014		0.020
D	4.45		4.95	0.175		0.194
E	3.30		3.94	0.130		0.155
e	2.41		2.67	0.094		0.105
e1	1.14		1.40	0.044		0.055
L	12.70		15.49	0.50		0.610
R	2.16		2.41	0.085		0.094
S1	0.92		1.52	0.036		0.060
W	0.41		0.56	0.016		0.022
V		5°			5°	



SOT23-3L MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.890		1.120	35.05		44.12
A1	0.010		0.100	0.39		3.94
A2	0.880	0.950	1.020	34.65	37.41	40.17
b	0.300		0.500	11.81		19.69
C	0.080		0.200	3.15		7.88
D	2.800	2.900	3.040	110.26	114.17	119.72
E	2.100		2.64	82.70		103.96
E1	1.200	1.300	1.400	47.26	51.19	55.13
e		0.950			37.41	
e1		1.900			74.82	
L	0.400		0.600	15.75		23.63
L1		0.540			21.27	
k			8°			8°



5 Revision history

Table 6. Document revision history

Date	Revision	Changes
09-Oct-2004	1	First document
22-Jun-2004	2	Complete document
06-Apr-2005	3	New typ and max value inserted for Vgs(th)
19-Apr-2005	4	New stylesheet
26-Apr-2005	5	New Pin Configuration for TO-92
28-Apr-2005	6	Pin configuration change again
19-Jun-2006	7	New template, no content change

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